1. (a) Planarization is an abrasive process using slurries and circular sanding action to polish the surface of the wafer, so the smooth surface maintained photolithographic depth of focus for the subsequent processing steps and insure the interconnects. (2%)
(b) Using the gate layer serving as a mask, self-alignment techniques used to solve the problem of maintaining relative alignment between different elements (gate, source/drain) of the photo-mask. (3%)
(c) Please refer to textbook section 2.3.1. (5%)

2. (a)  

(b)  

M1
Contact
Poly
P Diff
N Diff

(b)  

M1
Contact
Poly
P Diff
N Diff
(c) All P MOSs’ w/l ratio are 8/1 and 4/1 for the N-MOS have been labeled on the layout. (2%) If we increase/decrease the P-N W/L ratio, the output resistance will be decreased / increased (increase the P / N’s ratio, the cell pull-up / pull-down slop will get steeper). (5%)

3. M1 plate capacitance:
\[ \{[3 \times (0.5/2)] \times [12 \times (0.5/2)] + [4 \times (0.5/2)] \times [4 \times (0.5/2)]\} \times 0.04 = 0.13 \text{ (fF)} \]
M1 fringe capacitance:
\[ (3 + 12 + 4 + 4 + 4 + 1 + 12) \times (0.5/2) \times 0.09 = 0.9 \text{ (fF)} \]
N-Diff bottom capacitance:
\[ [6 \times 10] \times (0.5/2) \times (0.5/2) \times 0.6 = 2.25 \text{ (fF)} \]
N-Diff side-wall:
\[ [6 + 10 + 6 + 10] \times (0.5/2) \times 0.2 = 1.6 \text{ (fF)} \]
\[ C_{\text{in}} = 0.13 + 0.9 + 2.25 + 1.6 = 4.88 \text{ (fF)} \]
(10%).

Figure 2: