1. Please explain (21%):
   a. 超大型積體電路, Very Large Scale Integrated circuit (used to define the IC
      has more than 10,000 transistors, 3%)
   b. Refer to class notes: Chapter2, page 5 (3%).
   c. Refer to textbook section 2.3.4 please (6%)
   d. Voltage difference between output of one gate and input of next. Noise must
      exceed noise margin to make second gate produce wrong output (3%)
   e. The switch logics do not connect to the logic “H” or “L”. When the switch
      logic turns on, all the connected capacitors will re-distribute the charges to
      make all connected capacitors on the same voltage. The final voltage depends
      on the ratio of the capacitance, and could possible produce arbitrary voltage
      on intermediate nodes (3%).
   f. Flip-Flop cascades by two cascaded latches and is an edge triggered, non-
      transparent device. Latch is a transparent, level triggered device (3%).

2. 
   a. \( P_{w1} = 1 - P_{i1} \cdot P_{i2} = 1 - 0.5 \cdot 0.5 = 0.75 \); 
      \( P_{w2} = 0.75 \); 
      \( P_{w4} = 1 - (1 - (1 - P_{w1})(1 - P_{w2})) = 0.0625 \); 
      \( P_{w3} = 1 - (1 - (1 - P_{i6})(1 - P_{i7})) = 0.25 \); 
      \( P_e = 1 - P_{i5} \cdot P_{w3} = 1 - 0.5 \cdot 0.25 = 0.875 \); 
      \( P_{o1} = 1 - (1 - (1 - P_{w4}) \cdot (1 - P_e)) = 0.1171875 \) # 
      \( P_{o2} = 1 - P_e \cdot P_{i8} = 1 - (0.875 \cdot 0.5) = 0.5625 \) # (5%)
   b. \((i_1, i_2, i_3, i_4, i_5, i_6, i_7, i_8) = (0, x, x, x, 1, 0, 0, x)\) observe on O1, or
      \((x, x, x, x, 1, 0, 0, 1)\) observe on O2 (5%)?

3. a. Critical timing paths: \( i_1 \rightarrow O_1 \); 7 ns (2%).
   b. \( W_4 = (i_1 \cdot i_2 \cdot i_3 \cdot i_4) = i_1 \cdot (i_2 \cdot i_3 \cdot i_4) \)
      = \( i_1 \AND (i_2 \AND (i_3 \AND i_4)) \);
      The logic above reduced the arrival time of \( W_4 \) from 6 ns down to 5.5 ns and \( O_1 \)
      came out at 6.5 ns (5%)