1. Please explain (21%):
   a. What does VLSI stand (abbreviation) for (3%)?
   b. Draw a simplified foundry fabrication flow (from the layout, GDSII, to the wafer out. Don’t mess up with the photolithography flow. 3%)? Please mark if there is any iteration.
   c. What’s “Latch up” in the CMOS IC (3%)? How to prevent “Latch up” (3%)?
   d. What’s “Noise Margin” (3%)?
   e. What’s “Charge Sharing” in the switching logic (3%)?
   f. What are the differences between a static “Flip-Flop” and a “Latch” (3%)?

2. Please refer to Figure 1.
   a. If all the input signal probabilities are equal to 0.5 (the probability the signal will show as logic HIGH), what’s the probability of $O_1 / O_2$ equal to “1” (logic HIGH) (5%)?
   b. If point “e” (marked as x) stock at 1, SA1. Would you please find a set of the inputs to catch the SA1 on point “e” (5%)?

3. Please refer to Figure 1 again. If all two input NAND, NORD delay are 1 ns; AND, OR are 1.5 ns delay; from any inputs to the output, regardless the fan-out number and loading. An inverter has 0.5 ns delay. Inputs, $i_2 \sim i_8$ arrived at the same time (time 0), the $i_1$ arrived later than $i_2 \sim i_8$ for 4 ns (time 4 ns). Please point out the critical timing path (2%). Please show any method to speed up the timing on $O_1$ output and make the delay shorter than 7 ns, by using the gates mentioned above (5%).