Schedule

08. 04/13/17 Midterm Examination

09. 04/20/17 Review; Chapter 2 (Electro-Migration & RC ext)

10. 04/27/17 Chapter 2 (CMP & Design Rule)

11. 05/04/17 Chapter 3 (Logic Gates, Noise Margin, power)

12. 05/11/17 Chapter 3 (Fan-out and loading, timing)

13. 05/18/17 Chapter 4 (Simulation, Cross Talk)

14. 05/25/17 Quiz 2, Chapter 4 (ATPG & DFT)
Logic Level (Gate Level)

MOS Level ✔

Layout ✔

Cross-section ✔
Chapter 2: Transistors and RC

Wire and via structures

Metal Migration

Wire parasitic

Transistor parasitic
Wires and vias (plugs)

Stagger vias

contacts

via
Metal migration

Current-carrying capacity of metal wire depends on cross-section. Height is fixed, so width determines current limit. Metal migration: when current is too high, electron flow pushes metal atoms. Higher current density increases metal migration, leading to destruction of wire.
Metal migration problems and solutions

Marginal wires will fail after a small operating period—*infant mortality.* (bathtub)

Normal wires must be sized to accommodate maximum current flow:

\[ I_{\text{max}} = 1.5 \text{ mA/\textmu m} \]

Mainly applies to \( V_{\text{DD}}/V_{\text{SS}} \) lines. (one directional current flow)
Source/drain have significant capacitance, resistance.
Measured same way as for wires.
Source/drain R, C may be included in Spice model rather than as separate parasitics.
Parallel plate capacitance

Formula for parallel plate capacitance:

\[ C_{ox} = \varepsilon_{ox} \frac{A}{d}, \text{ for unit area} = \frac{\varepsilon_{ox}}{x_{ox}} \]

Permittivity of silicon:

\[ \varepsilon_{ox} = 3.46 \times 10^{-13} \text{ F/cm}^2 \]
MOSFET gate as capacitor

Basic structure of gate is parallel-plate capacitor:

 gate

\[ \text{SiO}_2 \]

substrate

\[ V_g \]

\[ x_{ox} \]
Basic transistor parasitics

Gate capacitance $C_g$. Determined by active area.

Source/drain overlap capacitances $C_{gs}$, $C_{gd}$. Determined by source/gate and drain/gate overlaps. Independent of transistor $L$.

$C_{gs} = C_{ol} \ W$

Gate/bulk overlap capacitance.
Basic transistor parasitics

Gate to substrate, also gate to source/drain.
Source/drain capacitance, resistance.
0.25 micron transistor (Bell Labs)

gate oxide

source/drain

silicide

poly
Transistor gate parasitics

Gate-source/drain overlap capacitance:

\[ C_{gd} \]

\[ C_{gs} \]

\[ C_g \]
Diffusion wire capacitance

Capacitances formed by p-n junctions:

- Sidewall capacitances
- Depletion region

- Bottom wall capacitance

Capacitances formed by p-n junctions:

- Depletion region capacitance
- Sidewall capacitances

substrate \( (N_A) \)

\( n^+ \) \( (N_D) \)
Depletion region capacitance

Zero-bias depletion capacitance:

\[ C_{j0} = \varepsilon_{si} / x_{d0}. \]

Depletion region width:

\[ x_{d0} = \sqrt{\left(\frac{1}{N_A} + \frac{1}{N_D}\right)^2 2\varepsilon_{si} V_{bi} / q}. \]

Junction capacitance is function of voltage across junction:

\[ C_j(V_r) = C_{j0} / \left(1 + V_r/V_{bi}\right)^2. \]
Poly/metal wire capacitance

Two components:
- parallel plate;
- fringe.
Metal coupling capacitances

Can couple to adjacent wires on same layer, wires on above/below layers:

![Diagram showing metal coupling capacitances](image)
Example: parasitic capacitance measurement

n-diffusion: bottom-wall + sidewall
metal: plate + fringe
Via/Cntct: ignored

VLSI Design : Chapter 2-2
Wire resistance

Resistance of any size square is constant:
Typical resistance values for 0.5 micron process

metal 3: 0.03 ohms/square
metal 2: 0.07 ohms/square
metal 1: 0.08 ohms/square
Poly: 4 ohms/square
ndiff: 2 ohms/square
pdiff: 2 ohms/square
Calculating resistance

Determine current flow, then aspect ratio:

2 \text{ vs. } 20

VLSI Design : Chapter 2-2 22
Current around corners

Resistance at corner of two equal-width wires is approximately 1/2 square:
Example: wire resistance

Total \( R \) = \( \rho_{\text{sq}} \times (3.5 + 0.5 + 2) = \rho_{\text{sq}} \times 6 \)
An example of resistance calculation

poly : $4 \text{ ohms} \times 5 = 20 \text{ ohms}$

pdiff: $2 \text{ ohms} \times (3+1/2+2) = 11 \text{ ohms}$
Resistors

- Goal to offer wider range of sheet resistance
  - Tradeoff between tolerance, TCR, matching, and $I_{DC}$

- BEOL TaN resistor
  - Provides good overall characteristics

<table>
<thead>
<tr>
<th>Resistor Type</th>
<th>Extra Mask</th>
<th>$R_s$ (Ohm/sq.)</th>
<th>$3\sigma$ Tol. (%)</th>
<th>TCR (ppm/°C)</th>
<th>Matching (%-um)</th>
<th>$I_{DC}$ (μA/μm)</th>
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<tr>
<td>P+ Polysilicon</td>
<td>0</td>
<td>260</td>
<td>15</td>
<td>160</td>
<td>5.0</td>
<td>0.5</td>
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<tr>
<td>Precision Poly</td>
<td>1</td>
<td>165</td>
<td>8</td>
<td>210</td>
<td>6.5</td>
<td>0.5</td>
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<tr>
<td>High Value P- Poly</td>
<td>1</td>
<td>1600</td>
<td>20</td>
<td>-1360</td>
<td>8.5</td>
<td>0.1</td>
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<tr>
<td>High Value P- Poly</td>
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<td>3800</td>
<td>25</td>
<td>-2500</td>
<td>11.0</td>
<td>0.1</td>
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<tr>
<td>Sub-C N+ Diffusion</td>
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<td>8.1</td>
<td>15</td>
<td>1460</td>
<td>20.0</td>
<td>1.0</td>
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<tr>
<td>N+ S/D Diffusion</td>
<td>0</td>
<td>63</td>
<td>10</td>
<td>1500</td>
<td>6.0</td>
<td>1.0</td>
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<tr>
<td>P+ S/D Diffusion</td>
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<td>14</td>
<td>1340</td>
<td>8.0</td>
<td>1.0</td>
</tr>
<tr>
<td>High Value Xtal</td>
<td>1</td>
<td>1750</td>
<td>15</td>
<td>300</td>
<td>6.2</td>
<td>1.0</td>
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<tr>
<td>TaN BEOL</td>
<td>1</td>
<td>61</td>
<td>6</td>
<td>-387</td>
<td>0.0</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Typical Values achieved in AMS Technologies
Via resistance

Determined by current flow through via cut.
Typical metal1-poly contact: 2.5 ohms.
Typical metal1-metal2 contact: 0.5 ohms.
MIM Capacitors

- Goal: High density with high reliability and low cost
- Dielectrics: Oxide $\rightarrow$ Nitride $\rightarrow$ Hi-K
- Structure: VNCAP

Vertical Native CAPacitor (VNCAP)
no added processing cost
1.8 fF/µm² in 130nm
2.0 fF/µm² in 90nm
Last Metals Options

Technology supports choice of three last metal options

Cadence kits configured for particular option

Version suffix ends in “AM”, “ML”, or “DM”

Diagram shows layer name and thickness in microns
Inductors

Goal: *Maximum Q and inductance density with minimal process addition*

- Lower series resistance by using thick top metals
- Increase dielectric thickness to reduce SX loss
- Faraday shield to reduce SX loss
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14. 05/25/17 Quiz 2, Chapter 4 (ATPG & DFT)
15. 06/01/17 Chapter 5 (Memory types, Set-up & hold time)
Chapter 2: Transistor & Layout

Planarization (CMP)
Fabrication & Design rules
Scalable design rules
Packaging
Planarization

(b) 稍微平坦化製程

(c) 部份平坦化製程

(d) 局部平坦化製程

(e) 晶片全面平坦化製程

圖 6.19 平坦化製程之定義（續）
Wiring problems

Variations in height.
Lack of planarity -> step coverage.
Planarization: for more metal layer
Planarization
CMP

圖 6-21  CMP 研磨機之結構圖
Chemical-Mechanical Planarization (CMP)

Polishing pad wear, slurry composition, pad elasticity make this a very difficult process step.
Area Fill

Area fill feature insertion
Decreases local density variation
Decreases the ILD thickness variation after CMP

Features

Area fill features

Post-CMP ILD thickness
VCMP
Integrated Analysis and Optimization

Virtual Chemical Mechanical Polishing (VCMP) analysis identifies metal and dielectric thickness variation hot spot, and guides dummy metal insertion to improve thickness uniformity throughout the chip.
Manufacturing problems

Photoresist shrinkage, tearing. Wave length.
Variations in material deposition.
Variations in temperature.
Variations in oxide thickness and quality.
Variations between lots.
Variations across a wafer/wafers.
Impurities.
Transistor problems

Variations in threshold voltage:
  - oxide thickness;
  - ion implantation;
  - poly variations.

Changes in source/drain diffusion overlap.

Variations in substrate.
Wiring problems

Diffusion: changes in doping -> variations in resistance, capacitance.

Poly, metal: variations in height, width -> variations in resistance, capacitance.

Shorts and opens:
Defect-related Yield

Manufacturing process may introduce some defects in the layout.

<table>
<thead>
<tr>
<th>Exposed</th>
<th>&quot;Defect-free proc.&quot;</th>
<th>&quot;Break&quot;</th>
<th>&quot;Short&quot;</th>
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<tbody>
<tr>
<td>Etching</td>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
<td><img src="image3.png" alt="Diagram" /></td>
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<tr>
<td>Str.</td>
<td><img src="image4.png" alt="Diagram" /></td>
<td><img src="image5.png" alt="Diagram" /></td>
<td><img src="image6.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

Wiring problems

Extrinsic defects:

1. Hillocks (or whisker) and voids:

2. Intrusions and extrusions:

3. Stringers:

4. Particle remnants:

5. Partially filled contacts/vias:
A chip
Poly burned-out was found.
Poly burned-out was found.
VIA problems

Via may not be cut all the way through.

Undersize via has too much resistance. (VIA’s air gap)

Via may be too large and create short.
圖 6-13 障礙層故障所形成之鎵火山
(a) 橫向之 TiN 障礙層被 WF₆ 氣體所侵入
(b) TiN 和 WF₆ 反應而造成 TiN 剝落
(c) W 沉積在剝落之 TiN 上面，而形成火山狀
(d) 良好沒有火山狀之製程示意圖
Processing Defects

- Particles
- Vias
- CMP
- Lithography
- Variations

Size Variations:
- 250 nm
- 180 nm
- 130 nm
- 90 nm
- 65 nm
- 45 nm
Why do we need design Rules

To be able to tolerate some level of fabrication errors such as

- Mask misalignment
- Dust
- Process parameters (e.g., lateral diffusion)
- Rough surfaces
Why we need design rules

Masks are tooling for manufacturing.
Manufacturing processes have inherent limitations
Design rules specify geometry of masks which will provide reasonable yields.
Design rules are determined by experience.
微塵所造成的缺點

A. 微塵位在線上 → 可能造成斷線  FAIL
B. 微塵位在線間 → 可能造成短路  FAIL
C. 微塵位在線邊緣 → 可能造成信賴度問題
Defect-layout relationship

Yield in terms of area and design rules

- Larger area → lower yield
- Smaller geometries → higher sensitivity to defects

⇒ trade-off: yield loss must be expressed in terms of the defect size and layout characteristics rather than in terms of area alone

More relaxed layout

More aggressive layout
Across-Wafer Frequency
Variations

Lot-to-lot (within a fab.)  Wafer-to-wafer (within a lot)  Die-to-die (within a wafer)  Device-to-device (within a die)

INTER-DIE VARIABILITY  INTRA-DIE VARIABILITY
Design Rules

Interface between designer and process engineer

Rules constructed to ensure that design works even when small fabrication errors (within some tolerance) occur

Guidelines for constructing process masks

Unit dimension: Minimum line width

scalable design rules: lambda parameter

absolute dimensions (micron rules)
## Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
Design Rules

Different Potential

Same Potential

Well

Active

Select

Polysilicon

Metal1

Contact or Via Hole

0 or 6

9

3

2

2

3

2

2

3

10
CMOS design rules
Design Rules

Well: Min width/ space
Active: Min width/space, (A)
        space with contacts (B)
        space with poly (C)
Poly/Wire: Min width/space (D, E)
          Min extension of poly (F)
          Min poly to active space (C)
Design Rules

Poly/Wire: Min poly active space (J)
Contact: Min/Max contact size
   Min contact poly space (G)
   Min contact Metal space (H)
   Min contact active space (I)
   Min contacts spacing
Design Rules Number

- 0.35um
- 0.25um
- 180nm
- 150nm
- 130nm
- 90nm

VLSI Design : Chapter 2-2
### Design Rule

<table>
<thead>
<tr>
<th>Type of layer</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-well</td>
<td>600</td>
<td>724</td>
<td>850</td>
<td>ohm/sq</td>
</tr>
<tr>
<td>N+</td>
<td>45</td>
<td>65</td>
<td>85</td>
<td>ohm/sq</td>
</tr>
<tr>
<td>P+</td>
<td>115</td>
<td>165</td>
<td>215</td>
<td>ohm/sq</td>
</tr>
<tr>
<td>Poly1</td>
<td>45</td>
<td>55</td>
<td>65</td>
<td>ohm/sq</td>
</tr>
<tr>
<td>Poly2</td>
<td>--</td>
<td>30</td>
<td>50</td>
<td>ohm/sq</td>
</tr>
</tbody>
</table>
λ and design rules

λ is ½ size of a minimum feature (gate length).

Specifying λ particularizes the scalable rules.

Parasitics are generally specified in λ units.

Following are some examples
Wires

- Metal 7
- Metal 2
- Metal 1
- Poly
- $p^+$ diff / $n^+$ diff
Transistors
Types of via: metal1/diff, metal1/poly, metal1/metal2.
Metal 3 via

Type: metal3/metal2.

Rules:
- cut: 3 x 3
- overlap by metal2: 1
- minimum spacing: 3
- minimum spacing to via1: 2
Well Contact (Tub tie)
Spacing

Diffusion/diffusion: 3
Poly/poly: 2
Poly/diffusion: 1
Via/via: 2
Metal1/metal1: 3
Metal2/metal2: 4
Metal3/metal3: 4
DR, Yield and Customer Complains

- Loosened Design Rule => Die Cost dropped
- Loosened Design Rule => Yield dropped
- Yield dropped => Good dice Cost raised
- Loosened Test Coverage => Yield raised => Profit raised;
  however, lost customer => Profit dropped
Corners

Different corner for the chip processes (split processes):

1. TT, HNLP, LNHP (Process corner)
2. TT, FF, SS (Temp, voltage have been included. However, ……. )
2-10 reference answer

Area = (0.25x2) x (0.25x15) = 1.875 (um^2)

Perimeter = (15x0.25 + 2x0.25) x 2 = 8.5 (um)

C = 0.09 x 1.875 + 0.03 x 8.5 = 0.4237 fF

R = 15/2 * 4 = 30 (Ohm)
Chapter 2:
2-14, 2-18