Schedule

05. 03/29/18 Quiz 1, Chapter 2 (Transistors)
06. 04/05/18 清明節
07. 04/12/18 Chapter 2 (Cross-section, latch up)
08. 04/19/18 Midterm Examination
09. 04/26/18 Review; Chapter 2 (Layout, Reverse Engineering)
10. 05/03/18 Chapter 2 (Electro-Migration & RC ext)
11. 05/10/18 Chapter 2 (CMP & Design Rule)
Midterm!! Next Week!!

35%

Covered From Chapter 1 to next week’s material

Please bring your photo ID and color pens

Seat will be assigned
Quick Look Again (1)

(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask
Quick Look Again (2)

(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{Tp}$ adjust implants

(f) After p-well and $V_{Tn}$ adjust implants
Quick Look Again (3)

(g) After polysilicon deposition and etch

(h) After n+ source/drain and p+ source/drain implants. These steps also dope the polysilicon.

(i) After deposition of SiO₂ insulator and contact hole etch.
Quick Look Again (4)

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO$_2$ insulator, etching of via’s, deposition and patterning of second layer of Al.
Real Device VS Layout
Transistor Layout

Figure 6.1 A typical layout of a transistor having nonshared junctions with contacts.
Figure 2.15  (a) A series connection of two transistors and (b) a possible layout.
Figure 6.2 A typical layout of a transistor having a shared junction without a contact.

Figure 6.3 A typical layout of a transistor having a shared junction with a contact.
CMOS Inverter

(a) Layout

(b) Cross-Section along A-A

Cross-section
An Inverter

Fig. 3.5 Creating an n-well for CMOS circuits.

Fig. 3.6 Self-aligned process of creating transistors for the inverter.
An Inverter-2

Fig. 3.7 Metallization process of a CMOS inverter.

Fig. 3.4 CMOS inverter: (a) transistor schematic; (b) composite layout; (c) top view; (d) cross sectional view.
IC Cross Section and 3D View
A Real Cross-section

N-通道 LDMOS 之基本結構圖
Examples

Fig. 3.18 Inverter symbolic layout and its stick diagram.

Fig. 3.21 Inverter symbolic layout with wider transistors.
Wafer Representation of Layout Polygons

Aerial or Layout View

Wafer Cross-sectional View
Fig. 3.22 Symbolic layout of a two-input NAND gate.

Fig. 3.23 An optimized symbolic layout of a 2-input NAND gate.
A stick diagram is a cartoon of a layout. Does show all components/vias (except possibly tub ties), relative placement. Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.
Stick layers

metal 3
metal 2
metal 1
poly
ndiff
pdiff
Dynamic latch stick diagram

VDD

in

c poly

VSS

φ'

φ

Metal

P diff

contact

out

N diff
Latch-up

CMOS ICs have parasitic silicon-controlled rectifiers (SCRs).

When powered up, SCRs can turn on, creating low-resistance path from power to ground. Current can destroy chip.

Early CMOS problem. Can be solved with proper circuit/layout structures.
Latch-up
Latch-up

Equivalent circuit

Fig. 4.38 Parasitic transistors of a CMOS logic.
Parasitic SCR structure

*Silicon Controlled Rectifier*
Solution to latch-up

Use well contacts (tub ties) to connect wells to power rail. Use enough to create low-voltage connections.
Solution to latch-up

Vss

poly

Reverse bias

poly

Vdd

P+

n+

p-well

n+

p+

n-well

P−

N+

Fig. 3.7 Metallization process of a CMOS inverter.
What is Latch-up?

**Latch-up:** CMOS中形成一個雜散的PNPN結構的SCR。當元件通過的電流，促使SCR導通，產生足以破壞CMOS的大電流。

**Avoidance methods:**
- Increase the distance of the discrete elements (Layout)
- Use guard ring (Layout)
- Reduce substrate resistance (ex: epi) (Process)
- SOI (Process)
- Retrograde well (Process)
- Trench isolation (Process)
Three Latch-up Must Conditions

(1) The pnpn path must exit.
(2) The triggering resource must be large enough to make the SCR turn on. ($\beta_{npn} \times \beta_{pnp} > 1$)
(3) Power supply voltage must be larger than the SCR holding voltage ($V_h$).
Latch-up Types

Internal Latch up
- Applied in the core parts
- There are no guard rings
- Latch-up resistant method: forbid triggering source larger than $V_t$
- Parasitic device have low $V_h$

External Latch up
- Applied in the I/O parts
- There are double guard rings.
- Parasitic devices have high $V_h$
- Latch up resistant method: power<$V_h$
Latch up Standards

- JEDEC EIA/JESD78D 電子工業協會 (2011.11)
- AEC-Q100-011-B 汽車電子協會
- Mil-883F = JESD78(A) 美國軍標等同 JESD78(A)
Latch up Test Methodology

- **I trigger:** for IO pins

---

**Latch-up test circuit (Positive current):**
- Connect to an input terminal, power source, or GND terminal.
- Output terminal is open.

**Latch-up test circuit (Negative current):**
- Connect to an input terminal, power source, or GND terminal.
- Output terminal is open.

**Graph:**
- Stress current for characterization
- Max. $V_{supply}$
- GND
- PIN
- PIN UNDER TEST
- Time: $T_1 \rightarrow T_2$, $T_4 \rightarrow T_7$
- Operation:
  - Measure nominal $I_{supply}$ (Ion)
  - Cool down time (Tcool)
  - Wait time prior to $I_{supply}$ measurement.
- Measure $I_{supply}$
- If any $I_{supply} >$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from DUT.
Latch up Test Methodology

- Over Volatge test (V trigger): for Power pins

Devices shall be tested with all input pins (including I/O) in the following conditions:
- Tied to logic high
- Tied to logic low

Stress voltage for characterization

Max. \( V_{\text{supply}} \)

GND

\( V_{\text{supply}} \)

PIN

\[ \text{Time} \quad \text{Operation} \]
\[ T1 \rightarrow T2 \quad \text{Measure nominal } I_{\text{supply}} \text{ (nom)} \]
\[ T4 \rightarrow T7 \quad \text{Cool down time } (T_{\text{cool}}) \]
\[ T4 \rightarrow T5 \quad \text{Wait time prior to } I_{\text{supply}} \text{ measurement} \]
\[ T5 \quad \text{Measure } I_{\text{supply}} \]
\[ T6 \quad \text{If any } I_{\text{supply}} \text{ exceeds the failure criteria defined in 1.3, latch-up has occurred and power must be removed from then on.} \]

NOTE: The wait time shall be sufficient to allow for power supply ramp down and stabilization of \( I_{\text{supply}} \).
Well Contact (Tub tie) layout

Well contact (Tub Tie)
Well Contact

Well contact (Tub Tie)

metal ($V_{DD}$)

n-well

n+
Threshold voltage

Components of threshold voltage \( V_t = V_{t0} + \Delta V_t \)

\[ V_{t0} = V_{fb} + \phi_s + Q_b/C_{ox} + V_{II} \]

\( V_{fb} = \) flatband voltage

\[ = \phi_{gs} - Q_f/C_{ox} \]

\( \phi_{gs} \) : depends on difference work function between gate and substrate

\( Q_f \) : trapped surface charge
Threshold voltage

\[ \phi_s = \text{surface potential} \]

Voltage on parallel plate capacitor. (function of doping concentration)

\[ V_{II} : \text{Additional ion implantation} \]
Threshold voltage (Body effect)

Reorganize threshold voltage equation:

\[ V_t = V_{t0} + \Delta V_t \]
\[ \Delta V_t = \gamma_n (\sqrt{\phi_s + V_{sb}}) - \sqrt{\phi_s} \]

\( V_{sb} \): source/substrate voltage \( V_{sb} \).
\( \gamma_n \): the body effect factor

\[ = (\sqrt{2q \varepsilon_{si} N_a})/C_{ox} \]
Gate voltage and the channel

\[ V_{ds} < V_{gs} - V_t \]

\[ V_{ds} = V_{gs} - V_t \]

\[ V_{ds} > V_{gs} - V_t \]
Sub-threshold current is an exponential function of gate voltage:

\[ \text{In} \, I_d = \text{subthreshold} \]

\[ V_G = 0 \, \text{V} \]
\[ V_D = 1.2 \, \text{V} \]
\[ V_B = 0 \, \text{V} \]
Leakage currents

Flow from source or drain to the substrate due to diode formed by junction.

General form of leakage current is given by diode law:

\[ I_l = I_{l0}(e^{qV_d/kt} - 1) \]
Oxide Defects

Amorphous structure of SiO₂:

The Si-SiO₂ Interface structure:

Note: the figures are 2-D projection of a 3-D structure.
Home works assignment

Chapter 1:
None

Chapter 2:
2-1, 2-9
6 STAGES OF TAKING AN EXAM UNPREPARED

DENIAL

FRUSTRATION

THE "DO RANDOM STUFF THE ANSWER MIGHT COME TO ME" STAGE

CHEATING ATTEMPT

DESPERATION

DEPRESSION AND REGRET

VIA 9GAG.COM
Midterm!! Next Week!!

35%

Covered From Chapter 1 to today’s material

Please bring your photo ID and color pens

Seat will be assigned
Schedule

08. 04/19/18 Midterm Examination

09. 04/26/18 Review; Chapter 2 (Layout, Reverse Engineering)

10. 05/03/18 Chapter 2 (Electro-Migration & RC ext)

11. 05/10/18 Chapter 2 (CMP & Design Rule)

12. 05/17/18 Chapter 3 (Logic Gates, Noise Margin, power)

13. 05/24/18 Chapter 3 (Fan-out and loading, timing)

14. 05/31/18 Chapter 4 (Simulation, Cross Talk)
Circuit Design

Layout

Process
Gate voltage and the channel

\[ V_{ds} < V_{gs} - V_t \]

\[ V_{ds} = V_{gs} - V_t \]

\[ V_{ds} > V_{gs} - V_t \]
The modern MOSFET

Features of deep submicron MOSFETs:
- epitaxial layer for heavily-doped channel;
- reduced area source/drain contacts for lower capacitance;
- lightly-doped drains to reduce hot electron effects;
- silicided poly, diffusion to reduce resistance.
SPICE MOSFET models

Simulation Program with Integrated Circuit Emphasis, SPICE 1975

Level 1: basic transistor equations of Section 2.2; not very accurate.
Level 2: more accurate model (effective channel length, etc.).
Level 3: empirical model.
Level 4 (BSIM): efficient empirical model.
New models: level 28 (BSIM2), level 53 (BSIM3)…… 56 , 63
SPICE Simulators

SPICE free simulator

OrCad PSPICE, HSPICE, I-SPICE, …… SPICE2

Fast SPICE (Piece-wise linear)
HSIM, NANOSIM (Synopsys),
UltraSIM (Cadence),
ADiT (Mentor)
Some Spice model parameters

$L$, $W$: transistor length, width.

$A_S$, $A_D$: source/drain areas.

(Refer to page 62 or any SPICE menu for more details)
Devices in the Design

MOS (provided by the foundry’s PDK)
Diode (provided by the foundry’s PDK)
Wire
R
C
L
Chapter 2 Transistors, Layout, and Reverse

Transistor structures

Basic transistor behavior
MOS

Transistor
Layout (佈局) 的工作?

Design – 抽象主義
Layout – 現實主義 (其實還是抽象)

將 RD 抽象的功能符號 - 轉化為具體可實行量產的工藝製具步驟, 是為 Layout 的主要工作, Layout 工作的好壞,攸關量產品的成本及良率.
Transmission gate circuit

Gate level

MOS level
Transmission gate layout (CMOS)
Layout Guideline

Symmetric!!

對稱!!
Device的方向性一致
MOS 對稱性

One-dimensional layout

Common axis of symmetry
Common-centroid layout
Isothermal

better

power devices

Noise

bad
Layout of Resistor

\[ R = R_s \left( \frac{L}{W} \right) \text{ohms} + 2R_{\text{contact}} \]
Layout of Resistor-2
## Resistor Type

Sheet Resistance Parameters (0.5um 5V 2P3M)

<table>
<thead>
<tr>
<th>Type of layer</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-well</td>
<td>600</td>
<td>724</td>
<td>850</td>
<td>ohm/sq</td>
<td>17~18%</td>
</tr>
<tr>
<td>N+</td>
<td>45</td>
<td>65</td>
<td>85</td>
<td>ohm/sq</td>
<td>30~31%</td>
</tr>
<tr>
<td>P+</td>
<td>115</td>
<td>165</td>
<td>215</td>
<td>ohm/sq</td>
<td>30~31%</td>
</tr>
<tr>
<td>Poly1</td>
<td>45</td>
<td>55</td>
<td>65</td>
<td>ohm/sq</td>
<td>18~19%</td>
</tr>
<tr>
<td>Poly2</td>
<td>--</td>
<td>30</td>
<td>50</td>
<td>ohm/sq</td>
<td>66%</td>
</tr>
</tbody>
</table>
Common Centroid Layout of Resistors
Layout of Capacitors

No fringing effect

\[ C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} W L \]

\[ C_{ox} \]
Fringe of Capacitance

MIM
PIP
MOS CAP

Substrate
MIM Capacitors

• Goal: High density with high reliability and low cost
  • Dielectrics: Oxide $\rightarrow$ Nitride $\rightarrow$ Hi-K
  • Structure: VNCAP

Vertical Native CAPacitor (VNCAP)
no added processing cost
1.8 fF/μm² in 130nm
2.0 fF/μm² in 90nm
Capacitor Type

Double poly (PIP)

A

poly2

poly1

n+

N-well

n+

Psub
MOS_Cap

A

B

Poly

N-well

Psub

p+  n+  n+  p+
Capacitor 對稱性

Common-Centroid Layout of Capacitor

- 利用 common centroid 來確保 capacitor ratio.
- 單位電容的 corner cut 45°及 dummy cap。目的是為減少製程的偏差。
Boundary Condition

(A)

(B)

維持佈局周遭環境的一致性，避免蝕刻時的過份侵蝕(Over etching)。
bad

better

MASK

more active

less active
Inductors

Goal: Maximum Q and inductance density with minimal process addition

- Lower series resistance by using thick top metals
- Increase dielectric thickness to reduce SX loss
- Faraday shield to reduce SX loss

\[ L = 0.7 \, \text{nH} \]
IC floor Plan

- Core: internal latch-up
- I/O: external latch up

*Power clamp uniform put in related of IO PAD.*
Fig. 8. The I/O cell layouts with: (a) double guard rings, (b) single guard ring, and (c) no guard ring, to investigate the compact layout rules for I/O cells.
Guard Rings

IO Cell
Guard Rings

Latchup at internal due to trigger at IO cells

Additional guard ring between IO and internal can significantly increase latch-up immunity.
Guard Rings

**IO to internal**

- P+
- N+
- PMOS
- Pick up
- Guard Ring

- I/O Circuits
  - PAD
  - 1-10

- Internal Circuits
  - P-substrate
  - NMOS
  - 2-3

- N-well
  - P+ N+
  - PMOS
  - 2-2

VLSI Design
Layout verification

DRC – Design Rule Checking
ERC – Electrical Rule Checking
LVS – Layout V.S. Schematic
LPE – Layout Parameter Extraction (RC Extraction)

Design Rule 由 foundry 提供, command file 由 foundry 或 cad 生成, 提供 layout/rd 做 verification (but with errors……)
Layout verification

LVS

Warning: Bad devices in layout.