Introduction to VLSI Design

Textbook:
Modern VLSI Design
IP-Based Design,
Third edition, Prentice Hall,
by: Wayne Wolf
This lecture will use

綜科館104
實驗室

Please noted
References

ULSI 製程技術 (新文京開發出版)
by: 劉博文

Digital Integrated Circuits
A Design Perspective

By: Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolić
Instructor

高得畬  Kao, De-Yu
E-mail: kao_deyu@yahoo.com

Class Notes:
http://www.cc.ntut.edu.tw/~dkao/

If possible, please down load the material right before the class……  :-p
Grading Policy

Two quizzes 30% (15% for each)
Midterm 35%
Final 35%
01. 02/23/17 Chapter 1 Introduction (Moore’s rule)
02. 03/02/17 Chapter 1 Introduction (Cost and TW)
03. 03/09/17 Chapter 2 (Mask)
04. 03/16/17 Chapter 2 (Processing)
05. 03/23/17 Chapter 2 (Transistors)
06. 03/30/17 Quiz 1, Chapter 2 (Cross-section, latch up)
07. 04/06/17 Chapter 2 (Layout, Reverse Engineering)
Schedule (2)

08. 04/13/17 **Midterm Examination**

09. 04/20/17 **Review; Chapter 2** (Electro-Migration & RC ext)

10. 04/27/17 **Chapter 2** (CMP & Design Rule)

11. 05/04/17 **Chapter 3** (Logic Gates, Noise Margin, power)

12. 05/11/17 **Chapter 3** (Fan-out and loading, timing )

13. 05/18/17 **Chapter 4** (Simulation, Cross Talk)
Schedule (3)

14. 05/25/17 Quiz 2, Chapter 4 (ATPG & DFT)
15. 06/01/17 Chapter 5 (Memory types, Set-up & hold time)
16. 06/08/17 Fin-FET
17. 06/15/17 Final Examination
18. 06/22/17 Exam review and more
Preview for Next Semester

Add-on   Packaging
Chapter 5 Sequential Machines (Memories)
Chapter 6 CPU / ALU, Data-path
Chapter 7 CAD
Chapter 8 Architecture
Chapter 9 Examples
Add-on   What’s next?
Time for the class
18:40
Questions ??.
Chapter One

Overview

VLSI?

Moore’s Law

The Difficulties in VLSI Design

Cost of the VLSI Design

Taiwan VLSI Related Industry
What’s VLSI

The definition in the 70~80’s
Fig. 1.1 Integration scales.

<table>
<thead>
<tr>
<th>Integration Scale</th>
<th>Number of Components</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSI</td>
<td>&lt; 10 transistors</td>
<td>Logic gates</td>
</tr>
<tr>
<td>MSI</td>
<td>10 - 1,000 transistors</td>
<td>Adders, counters</td>
</tr>
<tr>
<td>LSI</td>
<td>1,000 - 10,000 transistors</td>
<td>Multipliers</td>
</tr>
<tr>
<td>VLSI</td>
<td>&gt; 10,000 transistors</td>
<td>Microprocessors</td>
</tr>
</tbody>
</table>

VLSI: **Very Large Scale Integration.**

**Very Large Scale Integrated circuit.**

It basically means packing a large number of transistors (gates) into an integrated circuit die.

Another term: ULSI
電子元件

図 電阻

図 電容

図 二極體

図 電晶體
IC = 電阻 + 電容 + 二極體 + 電晶體
Where have you seen ICs?
Where have you seen ICs?
Why Silicon?

Abundant Element: 28% by weight in earth
Easily purified
Favorable electrical properties
Good mechanical, chemical, and thermal properties
Stable dopants available
Stable SiO₂ insulator, smooth, barrier
Why VLSI?

Integration improves the design:
- lower parasitics, higher speed
- lower power
- physically smaller
- lower cost

Integration reduces manufacturing cost-
(almost) no manual assembly.
Transistor – Bardeen (Bell Labs) in 1947
Bipolar transistor – Schockley in 1949
First bipolar digital logic gate – Harris in 1956
First commercial IC logic gates – Fairchild 1960
PMOS in 1960’s (calculators)
CMOS – 1960’s, but plagued with manufacturing problems
History

NMOS in 1970’s (4004, 8080) – for speed
CMOS in 1980’s – preferred technology
because of power benefits
Now, Copper (Low K), Hi-K, SOI, HiV…
Fin-FET

From left to right: Gordon Moore, C. Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni and Jay Last.
(1960) traitorous eight
BJT, nMOS, & CMOS

1949

bipolar

nMOS

CMOS

70’s

60’s
<table>
<thead>
<tr>
<th>Year</th>
<th>Bipolar</th>
<th>CMOS</th>
<th>III-V/Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>1980</td>
<td>49%</td>
<td>51%</td>
<td>~</td>
</tr>
<tr>
<td>1885</td>
<td>45%</td>
<td>55%</td>
<td>~</td>
</tr>
<tr>
<td>1990</td>
<td>30%</td>
<td>70%</td>
<td>~</td>
</tr>
<tr>
<td>1995</td>
<td>20%</td>
<td>79%</td>
<td>2%</td>
</tr>
<tr>
<td>2000</td>
<td>8%</td>
<td>88%</td>
<td>4%</td>
</tr>
</tbody>
</table>
Applications

Microprocessors:
  personal computers
  Microcontrollers
  Special-purpose processors
Memories (DRAM/SRAM).
Drivers (video displayers, motors, audio speakers, lights…. )
Hi-freq. PHY (TX/RX)
SOC, mixed mode, MEMS, Bio-Chips…….
IC 廣泛應用於各式各樣電子產品

Consumer

Computer

Communication

Car

Industrial

Military

Medicine
Pacemaker
沒有發明半導體的話

電腦的體積會～

無線手機的大小將～

ATLAS (2700個真空管)

真空管
Moore’s Law


In 1965, Moore predicted that number of transistors per chip would grow exponentially (double every 18 (24) months)

Exponential improvement in technology is a natural trend: steam engines, dynamos, automobiles…….
Moore’s Law

Fig. 1.2 Moore’s law.
Intel 4004

1 MHz clock (Intel 4004) – 1971
Intel 80386

275 K transistors
(Intel 80386) – 10/1985
Hi

History

Amazingly visionary – million transistor/chip barrier was crossed in the 1980’s.

- 2300 transistors, 1 MHz clock (Intel 4004) – 1971
- 134 K transistors (Intel 80286) – 2/1982
- 275 K transistors (Intel 80386) – 10/1985
- 1.2 Million transistors (Intel 80486) – 4/1989
- 3.1 Million transistors (Pentium) – 3/1993
- 5.5 Million transistors (Pentium Pro) – 11/1995
- 42 Million, 2 GHz clock (Intel P4) - 2001
- 1.7 Billion transistor (Intel Itanium 2) - 2006
- 5 Billion transistor (Intel Xeon Phi) - 2012
Intel Pentium IV

42 Million, 2 GHz clock (Intel P4) - 2001
Core 2 Duo

65nm, 6MB RAM, 4 GHz clock (Intel) – 2008 Jan.
Apple A6

32nm, 1.3 GHz clock
(Apple) –
2012 Sep.
Used in iPhone5

VLSI Design
Graphical illustration of Moore’s law

Something that doubles frequently grows more quickly than most people realize!

A 2002 chip can hold about 15,000 1981 chips inside itself
Progression
技術越先進，產出dice越多

100個晶粒

？個晶粒

7.5μm

1μm

VLSI Design
半導體技術進步促成產品價格的降低

年度          每一元美金所能買到的電晶體數量

1968年        1個

1985年        3,000個

2003年        50,000,000個
CPU
Memory

Human memory
Human DNA

4X growth every 3 years!

Year

Kbit capacity/chip
M 100 1,000 10,000 100,000 1,000,000 10,000,000
T 100 1,000 10,000 100,000 1,000,000 10,000,000

Page
1.6-2.4 μm

Book
1.0-1.2 μm

Encyclopedia
2 hrs CD audio
30 sec HDTV

Chip
0.13 μm
0.18-0.25 μm
0.35-0.4 μm
0.7-0.8 μm
0.9-0.6 μm
0.09 μm
0.065 μm
0.05-0.06 μm
Die Size

~7% growth per year
~2X growth in 10 years

Year

Die size (mm)

VLSI Design
Clock Frequency

Lead microprocessors frequency doubles every 2 years

- Something that doubles frequently grows more quickly than most people realize!
Lead Microprocessors power continues to increase

Power delivery and dissipation will be prohibitive

VLSI Design

Courtesy, Intel
Processor and Memory

Technology Roadmap in Processor and DRAM, Flash Memory

Power Performance for Application Processor Architecture, 2015

- Intel
- ARM
- MIPS
- Octo core >2GHz, 14nm
- Quad core 2GHz, 22nm
- Dual core 1.2GHz, 45nm
- Single core 1GHz, 65nm
- High
- Low

Performance

Power Consumption

Flash and DRAM Production ½ Pitch: Near-term Year

- Big challenges will be encountered as the technology node under 16nm in DRAM and NAND Flash manufacturing.
Rising on the Horizons

The Pace of Advanced Technologies Fueling Moore’s Law for Years to Come

- V_{dd} 1.0/1.1V 0.9/1.0V 0.8/0.9V 0.7/0.8V 0.6/0.7V 0.5/0.6V < 0.5V
- Process-induced Strain Engineering
- Advanced Gate Stack Engineering
- Fully-depleted Channel Electrostatics
- Band-Engineered Channel for Enhanced Transport
- New Transport & Extreme Channel Electrostatics
- Novel Materials
- Spintronics

Tech Node... 32/28nm 14nm 7nm 5nm 45nm 22/20nm 10nm
More Moore’s

The Novel Materials, Devices and Equipment Come with The Nodes & Transition of 450mm
First 3.2-Million Gate Virtex-EA FPGA

XCV3200EA manufactured by UMC’s 0.15um process

- Fab 8” 0.15um CMOS
- 1.8V Core, 3.3V I/O
- 1P/6LM, Dual-gate Oxide
- 225 Million Transistors
- 3.2M Gate-Count FPGA
- Top 2 Cu Layers to be Offered

Courtesy of Xilinx, Inc.
Wafer Size

2”, 3”, and 5”
1987, 6” (150mm)
1991, 8” (200mm)
1999, 12” (300mm)
2007, 18” (450mm)

More die per wafer, low cost

Most costly for new fab
**Bigger Wafer Size - Higher productivity**

<table>
<thead>
<tr>
<th>Unit Productivity Comparison</th>
<th></th>
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<tbody>
<tr>
<td><strong>Wafer Size</strong></td>
<td>1</td>
</tr>
<tr>
<td><strong>Gross Die</strong></td>
<td>1</td>
</tr>
</tbody>
</table>

晶圆越大，产出**dice**越多

8” wafer

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<th>2</th>
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<tbody>
<tr>
<td>3</td>
<td>4</td>
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</table>

12” wafer

<table>
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<tr>
<td>3</td>
<td>4</td>
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</tbody>
</table>

VLSI Design
Example: Foundry Capacity

TSMC produces 30K 8” wafer/month 2Q02
南科 joint the production line @ 4Q02 10K
12” wafer/ month

The total capacity will equal to
30K + 10K * (12 / 8)^2 = 52.5 K 8” wafer /mo
## Tech Roadmap

<table>
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<tbody>
<tr>
<td>Technology node [nm]</td>
<td>180</td>
<td>162</td>
<td>130</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>30</td>
</tr>
<tr>
<td>Supply [V]</td>
<td>1.5-1.8</td>
<td>1.5-1.8</td>
<td>1.2-1.5</td>
<td>0.9-1.2</td>
<td>0.6-0.9</td>
<td>0.5-0.6</td>
<td>0.3-0.6</td>
</tr>
<tr>
<td>Wiring levels</td>
<td>6-7</td>
<td>6-7</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>9-10</td>
<td>10</td>
</tr>
<tr>
<td>Max freq [GHz], Local-Global</td>
<td>1.2</td>
<td>1.6-1.4</td>
<td>2.1-1.6</td>
<td>3.5-2</td>
<td>7.1-2.5</td>
<td>11-3</td>
<td>14.9-3.6</td>
</tr>
<tr>
<td>Max µP power [W]</td>
<td>90</td>
<td>106</td>
<td>130</td>
<td>160</td>
<td>171</td>
<td>177</td>
<td>186</td>
</tr>
<tr>
<td>Bat. power [W]</td>
<td>1.4</td>
<td>1.7</td>
<td>2.0</td>
<td>2.4</td>
<td>2.1</td>
<td>2.3</td>
<td>2.5</td>
</tr>
</tbody>
</table>

**Node:** 2012/28nm; 2014/20nm; 2017/14nm running
A Real Case (UMC)
We will have all our lectures in

綜科館104實驗室

Please noted
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18. 06/22/17 **Exam review** and more

In 1965, Moore predicted that number of transistors per chip would grow exponentially (double every 18 (24) months).

Exponential improvement in technology is a natural trend: steam engines, dynamos, automobiles…….
Moore’s Law

Fig. 1.2 Moore’s law.
Technology Scaling

Gate Length (nm)


year

10,000 1,000 100 10 1

Increasing Technology Difficulty

DRAM 1.4 Times/Year

1TB (2023)

Neuron Number in Brain

64GB (2015)

1TB

64

1000

1.4

1014

1015

Transistor Number per chip

Increasing Technology Difficulty

VLSI Design
Power Density

![Graph showing the trend of power density over the years from 1970 to 2010. The graph includes data points for different processors, such as 8086, 386, 486, and Pentium® proc. The y-axis represents power density (W/cm²) on a logarithmic scale, and the x-axis represents the year.](image-url)
The Path to 90nm and Beyond

- Leakage
- Via Failures
- Variations
- Random Defects
- Cu Dishing, Erosion
- Printability Errors

Yield Loss
Software costs overtake total hardware costs at 130nm
# Energy Storage

<table>
<thead>
<tr>
<th>Material</th>
<th>KWH/kg</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gasoline</td>
<td>14</td>
</tr>
<tr>
<td>Lead-Acid</td>
<td>0.04</td>
</tr>
<tr>
<td>Li polymer</td>
<td>0.15</td>
</tr>
</tbody>
</table>
Battery

The graph shows the trend in energy density (Wh/kg) for various battery types over time, with the first commercial use timeline. Key dates and types include:

- **NiCd**
- **SLA**
- **NiMH**
- **Li-Ion**
- **Reusable Alkaline**
- **Li-Polymer**

The trend line indicates a significant increase in energy density from the 1940s to the 2010s, highlighting advancements in battery technology.
**Most Concerned Problem (Taiwan)**

<table>
<thead>
<tr>
<th>Rank</th>
<th>Problem Description</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>缩短設計週期</td>
<td>59.0%</td>
</tr>
<tr>
<td>2</td>
<td>降低設計成本</td>
<td>55.1%</td>
</tr>
<tr>
<td>3</td>
<td>IP驗證</td>
<td>19.2%</td>
</tr>
<tr>
<td>4</td>
<td>EMI</td>
<td>14.1%</td>
</tr>
<tr>
<td>5</td>
<td>類比IC佈局</td>
<td>11.5%</td>
</tr>
<tr>
<td></td>
<td>IP可用性</td>
<td>11.5%</td>
</tr>
<tr>
<td>6</td>
<td>類比模擬( SPICE)</td>
<td>10.3%</td>
</tr>
<tr>
<td></td>
<td>IP再使用</td>
<td>10.3%</td>
</tr>
<tr>
<td></td>
<td>電源管理</td>
<td>10.3%</td>
</tr>
<tr>
<td>7</td>
<td>RF設計</td>
<td>9.0%</td>
</tr>
<tr>
<td>8</td>
<td>ASIC模擬/快速原型建立</td>
<td>6.4%</td>
</tr>
<tr>
<td></td>
<td>混合訊號模擬</td>
<td>6.4%</td>
</tr>
<tr>
<td></td>
<td>熱管理</td>
<td>6.4%</td>
</tr>
<tr>
<td>9</td>
<td>佈局和佈線</td>
<td>5.1%</td>
</tr>
<tr>
<td></td>
<td>訊號完整性</td>
<td>5.1%</td>
</tr>
<tr>
<td>10</td>
<td>設計工具相容性</td>
<td>3.8%</td>
</tr>
<tr>
<td></td>
<td>實體合成</td>
<td>3.8%</td>
</tr>
<tr>
<td></td>
<td>實體驗證</td>
<td>3.8%</td>
</tr>
</tbody>
</table>

資料來源：電子工程專輯/2006年IC設計調查
SoC Design Challenges
Open Issues

Microscopic issues
- ultra-high speeds
- power dissipation and supply rail drop
- growing importance of interconnect noise, crosstalk
- reliability, manufacturability
- clock distribution

Macroscopic issues
- time-to-market
- design complexity (billions of gates)
- high levels of abstractions
- reuse and IP, portability
- systems on a chip (SoC)
- tool interoperability

<table>
<thead>
<tr>
<th>Year</th>
<th>Tech.</th>
<th>Complexity</th>
<th>Frequency</th>
<th>3 Yr. Design Staff Size</th>
<th>Staff Costs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1997</td>
<td>0.35</td>
<td>13 M Tr.</td>
<td>400 MHz</td>
<td>210</td>
<td>$90 M</td>
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<tr>
<td>1998</td>
<td>0.25</td>
<td>20 M Tr.</td>
<td>500 MHz</td>
<td>270</td>
<td>$120 M</td>
</tr>
<tr>
<td>1999</td>
<td>0.18</td>
<td>32 M Tr.</td>
<td>600 MHz</td>
<td>360</td>
<td>$160 M</td>
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<tr>
<td>2002</td>
<td>0.13</td>
<td>130 M Tr.</td>
<td>800 MHz</td>
<td>800</td>
<td>$360 M</td>
</tr>
</tbody>
</table>
Cost: about $15~20 billion USD. *

Typical fab line occupies about 1 city block, employs a few hundred people.

Most profitable period is first 18 months-2 years. (This might not be true)

* Nicolas Mokhoff
Semi industry fab costs limit industry growth
10/3/2012
Fab Cost

Source: Goldman Sachs

VLSI Design
Mask cost

**Semiconductor Wafer Mask Costs**

*September 15, 2016, anysilicon*
MOSIS MPW Program

- Winning Enabler for New Designs (Multi- Project- Wafer)
- MOSIS engagement model for start-ups and initial prototyping runs
- Validate IBM Model to Hardware Correlations and Tech Support on test chips

Foundry Mosis MPW Program
MOSIS Handle MPW runs for all IBM's generally available foundry technologies

MOSIS
- Full Information Available on www.MOSIS.com
  - Schedule, Pricing, Tech Availability
  - Flexible die size, quantity and packaging options
  - Frequent Regular MPW Schedule

Technology Availability
- SiGe BiCMOS
  - 0.13 (8HP)
  - 0.18 (7WL, 7HP)
  - 0.25 (6HP, 6DM)
  - 0.35 (5HE)
  - 0.5 (5DM, 5AM, 5PA, 5HP)
- CMOS
  - 0.13 (8RF-LM, 8RF-DM)
  - 0.18 (7SF, 7RF)
  - 0.25 (6RF)

MOSIS Information Science Institute
University of Southern California
4676 Admiralty Way, 7th Floor
Marina del Rey, CA 90292-6695

U.S. Rep: Wes Hansford
hansford@mosis.org
1-310-448-9316
2006 MOSIS MPW Schedule and Deliverables

A) MOSIS Deliverable = **40 dies** per each chip design

B) MOSIS MPW Pricing available at
http://www.mosis.org/Orders/Prices/price-list-export.html

<table>
<thead>
<tr>
<th>IBM BiCMOS SiGe</th>
<th>Jan</th>
<th>Feb</th>
<th>Mar</th>
<th>Apr</th>
<th>May</th>
<th>Jun</th>
<th>Jul</th>
<th>Aug</th>
<th>Sep</th>
<th>Oct</th>
<th>Nov</th>
<th>Dec</th>
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<tbody>
<tr>
<td>8HP 0.13</td>
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<td>27</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>9</td>
<td></td>
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<tr>
<td>7WL 0.18</td>
<td></td>
<td>23</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td>11</td>
<td>6</td>
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<td>7HP 0.18</td>
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<td>13</td>
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<tr>
<td>6HP 0.25</td>
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<td>5HPE 0.35</td>
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<tr>
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</tr>
<tr>
<td>5HP/5AM 0.50</td>
<td></td>
<td>9</td>
<td>8</td>
<td>18</td>
<td></td>
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</table>

See Taxi Runs for additional IBM run dates.

<table>
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<th>IBM CMOS</th>
<th>Jan</th>
<th>Feb</th>
<th>Mar</th>
<th>Apr</th>
<th>May</th>
<th>Jun</th>
<th>Jul</th>
<th>Aug</th>
<th>Sep</th>
<th>Oct</th>
<th>Nov</th>
<th>Dec</th>
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<tr>
<td>9RF 90 nm</td>
<td></td>
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<td></td>
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<td>27</td>
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<td>13</td>
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<td></td>
<td>7</td>
<td></td>
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<tr>
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<td>21</td>
<td>17</td>
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<td>21</td>
<td>16</td>
<td>4</td>
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<td>10</td>
<td>24</td>
<td>30</td>
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<td></td>
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</tr>
</tbody>
</table>

See Taxi Runs for additional IBM run dates.

http://www.mosis.org/products/fab/schedule/
http://www.mosis.org/Orders/Prices/price-list-export.html
Tool Cost

Workstation: 1.5K USD
Simulator: 1 ~ 10K USD (rented)
Synthesizer: 100K USD (rented)
Static Timing Check: 70K USD (rented)
Back-end Layout Tools: Couple M USD (rented)
Testers: 10 ~ M USD

Logic analyzer, FPGA, PCB, OSC scope, FG, curve tracer, testing load board, probe card, ……
Development Costs

Assumptions: 6M → 70M transistors, 3 mask spins, 250K Units.
**Dice / Wafer**

- **Wafer Size:** 8 inches
- **Die Size:** 8.841x2.252 (mm)
- **Number of Dies X (field):** 2
- **Number of Dies Y (field):** 11
- **Gross dice Forecast:** 1345
- **X Offset Value:** 7 mm
- **Y Offset Value:** -4 mm
- **Notch Reserved Distance:** 9 mm
- **Ring Edge Reserved Distance:** 3 mm
- **Alignment Mark Position (X):** 77.8 mm
- **Alignment Mark Position (Y):** 54.5 mm
- **Alignment Mark Tolerant Distance:** 1.6 mm
Costs (1)

Chip cost = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final yield number (good chips)}}

\text{cost of die} = \frac{\text{cost of wafer}}{\text{dice per wafer} \times \text{yield}}

\text{dice per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} = \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}

You can find different equations for the die number per wafer.

Experiences term

Dice 越小，產出良率越高
Clustered VLSI Defects

Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77
Enter die height: 2.221 mm
Enter die width: 1.484 mm
Enter edge exclusion: 5.0 mm
Select wafer size: 150 mm

Gross Die: 4,465
Enter defect density: 1.00 /cm²
Select yield model: Murphy
Yield: 96.8%

Net Die: 4,320

Note: Gross do not take into die lost to test alignment.
Wafer Map

Bad die
<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Defects/cm²</th>
<th>Area (mm²)</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>PowerPC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super SPARC</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
Design for Manufacturability (DFM)

Approaches

1) Worst-Case Approach: choose the SPICE model giving the worst possible behavior
   - Traditional choice is pessimistic and lead to circuit overdesign (neglects any kind of correlation)
   - Other techniques to choose the SPICE model values (accounting for correlation)

2) Probability Density Function Approach: keep track of the whole distribution
   - Expensive: need smart ways to do it
Die Cost = \[\text{dies per wafer} \times \text{yield}\]

Cost is a variable!!
Cost per IC

\[ \text{Cost per IC} = \text{Floating Cost} + \left( \frac{\text{Fixed Cost}}{\text{Volume}} \right) \]
Cost Factors in ICs

For large-volume ICs (floating cost):

Floating cost dominated the price; which included: die cost; packaging and testing (related expanses).

For low-volume ICs (fix cost),

design costs is the major concerns engineer and tools (hardware, software, ……)
Tapeout (mask, tooling)
Total Chip Cost

Floating Cost
- wafer + testing + packaging……

Fixed Cost
- Tools + engineering + demo system + shuttles
  + ……

$\begin{array}{l}
\text{quantities} \\
0 \quad \quad \quad 3M
\end{array}$
Changes technologies

Different technologies

Floating Cost
wafer + testing + packaging……

Tools + engineers + demo system + shuttle……

Fixed Cost

$ quantities

VLSI Design
Sales vs. Costs

Sales revenue

Company A

Balance point

profit

Floating Cost

loss

Fix Cost

quantities

0

3M

VLSI Design
Competitions

$\text{Sales revenue}$

$\text{Company A}$

$\text{Sales revenue}$

$\text{Company B}$

$\text{Delay}$

$0$ $3M$

$\text{quantities}$

$\text{VLSI Design}$
A reasonable result

![Graph showing sales revenue and delay for Company A and Company B]
Marketing survey
Specification

Design:
Architecture, Logic, Circuit
Backend, ....

 Manufacture:
Masks, Die, Packaging

Testing

Market
Design Cycle

Specification: function, cost, market window, etc.
Architecture: large blocks partition
Logic: gates + registers (memories)
Circuits: transistors, sizes for speed, power…
Backend design: Put the circuit on silicon, determines parasitics
Manufacture
Testing
A Simplified Design Flow

1. Marketing survey specification
   - English
   - Design: Architecture, Logic, Circuit Backend, ...,
2. GDSII
3. Manufacture: Masks, Die, Packaging
4. Chip
5. Testing

System Design
- RTL Design
  - Synthesis
    - Gate Level
      - Virtual Prototype
        - Place and Route
          - RC Extraction
            - Transistor CKT
              - GDSII

C, System-C, programs
- RTL, Verilog, VHDL
- EDIF, Verilog

Verify and Debug

Timing
- SPICE
  - Physical
    - SPICE

VLSI Design
Design Validation

Must check at every step that errors haven’t been introduced—the longer an error remains, the more expensive it becomes to remove it.

Forward checking: compare results of less- and more-abstract stages.

Back annotation: copy performance numbers to earlier stages.
Not the same as design validation: just because the design is right doesn't mean that every chip coming off the line will be right. Must quickly check whether manufacturing defects destroy function of chip. Must also speed-grade.
## Company Size

<table>
<thead>
<tr>
<th>Size</th>
<th>IC 墨設計工程師人數</th>
<th>總員工數</th>
</tr>
</thead>
<tbody>
<tr>
<td>10人以下</td>
<td>16.7%</td>
<td>3.8%</td>
</tr>
<tr>
<td>11~20人</td>
<td>28.2%</td>
<td>7.7%</td>
</tr>
<tr>
<td>21~30人</td>
<td>14.1%</td>
<td>9.0%</td>
</tr>
<tr>
<td>31~40人</td>
<td>5.1%</td>
<td>7.7%</td>
</tr>
<tr>
<td>41~50人</td>
<td>3.8%</td>
<td>9.0%</td>
</tr>
<tr>
<td>51~60人</td>
<td>10.3%</td>
<td>3.8%</td>
</tr>
<tr>
<td>61~70人</td>
<td>2.6%</td>
<td>1.3%</td>
</tr>
<tr>
<td>71~80人</td>
<td>1.3%</td>
<td>5.1%</td>
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<tr>
<td>81~90人</td>
<td>1.30%</td>
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</tr>
<tr>
<td>91~100人</td>
<td>0%</td>
<td>7.7%</td>
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<tr>
<td>101~200人</td>
<td></td>
<td>17.9%</td>
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<tr>
<td>201~500人</td>
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<td>11.5%</td>
</tr>
<tr>
<td>500人以上</td>
<td></td>
<td>9.0%</td>
</tr>
</tbody>
</table>

資料來源：電子工程專輯/2005年 IC 設計調查
Productivity

58%/Yr. compounded Complexity growth rate

21%/Yr. compound Productivity growth rate

Logic Tr./Chip
Tr./Staff Month.
The mythical man-month

The situation is even worse than the productivity gap indicates. In theory, adding designers to team reduces project completion time. In reality, productivity per designer decreases due to complexities of team management and communication. In the software community, known as “the mythical man-month” (Brooks 1975), at some point, can actually lengthen project completion time! (“Too many cooks”)

1M transistors, 1 designer=5000 trans/month
Each additional designer reduces for 100 trans/month
So 2 designers produce 4900 trans/month each

VLSI Design
Time to Market

The impact of being late to market is becoming more significant

Source: Semico Research
Time to Market

- Peak revenue
- Peak revenue from delayed entry
- On-time
- Delayed
- Market rise
- Market fall
- Quantities (M)
- Revenues ($) vs. Time (months)
- Costs ($) vs. Time
- On-time entry
- Delayed entry
- D
A reasonable result

Sales revenue

Company A

Company B

Delay

403x403

$
Conclusions

It’s a very tough business!!
Semiconductor Industry Segments

Design Houses:
  Fabless: Broadcom, Xilinx, PMCS, nVedia, (300+ in SV)… SunPlus, MediaTek, (250+ in TW)…
  IP Vendors: ARM, MIPS, eMemory, …
Pure Foundries: TSMC, UMC, Chartered, …
CAD: Synopsys/Avant!, Cadence, Mentor Graphics, … Syntest, Spring Soft/NOVA
Packaging: ASE (日月光), Amkor,
Equipment: Applied Material. HP, LAM
Fig. 1.3 Relationship between a silicon foundry, an IC design team, and a CAD tool provider.
Taiwan’s Semiconductor Industry Supply-Demand Chain Structure

IP
EDA
IC design
IC fabrication
Masking
Wafer
Substrate
Lead frame
Packaging
Testing


TMC, DuPont, TCE, PSMC

TSMC, UMC, VIS, Episil, AMPI, PSC, Mosel, Winbond, Nanya, Inotera Memories, LITE-ON, ProMos

ASE, ChipMOS, GreaTek, GTM, PowerTech, ASE, Lingsen, Sigurd, XinTec

ASE, ChipMOS, GreaTek, GTM, PowerTech, ASE, Lingsen, Sigurd, XinTec, KYEC, VisEra

Goyatek, eMemory, Faraday, Global
SpringSoft, Integrated Service
MEMC, Episil, Shin-Etsu Silicone, Taiwan, Utitech
Kinsus Interconnect, Nanya, Phoenix Precision
Fu-Seng, SDI, CanMore
Foundry Clients Analysis

![Bar Chart]

- **Fabless**
- **IDM**
- **System/ OEM**

<table>
<thead>
<tr>
<th>Year</th>
<th>Fabless</th>
<th>IDM</th>
<th>System/ OEM</th>
</tr>
</thead>
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<tr>
<td>2001</td>
<td>58%</td>
<td>36%</td>
<td>6%</td>
</tr>
<tr>
<td>2002</td>
<td>60%</td>
<td>35%</td>
<td>5%</td>
</tr>
<tr>
<td>2003</td>
<td>58%</td>
<td>37%</td>
<td>5%</td>
</tr>
<tr>
<td>2004</td>
<td>56%</td>
<td>38%</td>
<td>6%</td>
</tr>
<tr>
<td>2005</td>
<td>56%</td>
<td>39%</td>
<td>5%</td>
</tr>
<tr>
<td>2006</td>
<td>57%</td>
<td>38%</td>
<td>5%</td>
</tr>
<tr>
<td>2007</td>
<td>54%</td>
<td>39%</td>
<td>6%</td>
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</table>
2011 Top 20 Fabless Design Houses

<table>
<thead>
<tr>
<th>Rank</th>
<th>Company</th>
<th>HQ</th>
<th>2011 ($M)</th>
<th>% change 2010/2011</th>
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<tbody>
<tr>
<td>1</td>
<td>Qualcomm</td>
<td>U.S.</td>
<td>9910</td>
<td>38</td>
</tr>
<tr>
<td>2</td>
<td>Broadcom</td>
<td>U.S.</td>
<td>7160</td>
<td>9</td>
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<tr>
<td>3</td>
<td>AMD</td>
<td>U.S.</td>
<td>6568</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>Nvidia</td>
<td>U.S.</td>
<td>3939</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>Marvell</td>
<td>U.S.</td>
<td>3445</td>
<td>-4</td>
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<td>6</td>
<td>MediaTek</td>
<td>Taiwan</td>
<td>2969</td>
<td>-17</td>
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<tr>
<td>7</td>
<td>Xilinx</td>
<td>U.S.</td>
<td>2269</td>
<td>-2</td>
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<td>Altera</td>
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<td>9</td>
<td>LSI Corp</td>
<td>U.S.</td>
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<td>26</td>
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<td>Avago</td>
<td>Singapore</td>
<td>1341</td>
<td>13</td>
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<tr>
<td>11</td>
<td>Mstar</td>
<td>Taiwan</td>
<td>1220</td>
<td>15</td>
</tr>
<tr>
<td>12</td>
<td>Novatek</td>
<td>Taiwan</td>
<td>1198</td>
<td>4</td>
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<td>13</td>
<td>CSR</td>
<td>Europe</td>
<td>845</td>
<td>5</td>
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<td>14</td>
<td>ST-Ericsson</td>
<td>Europe</td>
<td>825</td>
<td>-28</td>
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<tr>
<td>15</td>
<td>Realteck</td>
<td>Taiwan</td>
<td>742</td>
<td>5</td>
</tr>
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<td>16</td>
<td>HiSilicon</td>
<td>China</td>
<td>710</td>
<td>9</td>
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<td>17</td>
<td>Spreadtrum</td>
<td>China</td>
<td>674</td>
<td>95</td>
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<td>18</td>
<td>PMC-Sierra</td>
<td>U.S.</td>
<td>654</td>
<td>3</td>
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<td>19</td>
<td>Himax</td>
<td>Taiwan</td>
<td>633</td>
<td>-2</td>
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<tr>
<td>20</td>
<td>Lantiq</td>
<td>Europe</td>
<td>540</td>
<td>-2</td>
</tr>
</tbody>
</table>

Sources: IC Insights
# 2016 Top 20 IC makers

## 1Q16 Top 20 Semiconductor Sales Leaders
($M, Including Foundries)

<table>
<thead>
<tr>
<th>Rank</th>
<th>1Q16 Rank</th>
<th>Company</th>
<th>Headquarters</th>
<th>1Q15 Tot Semi</th>
<th>1Q16 Tot Semi</th>
<th>1Q16/1Q15 % Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Intel*</td>
<td>U.S.</td>
<td>12,067</td>
<td>13,115</td>
<td>9%</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Samsung</td>
<td>South Korea</td>
<td>9,336</td>
<td>9,340</td>
<td>0%</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>TSMC (1)</td>
<td>Taiwan</td>
<td>6,995</td>
<td>6,122</td>
<td>-12%</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>Broadcom Ltd. (2)*</td>
<td>Singapore</td>
<td>3,679</td>
<td>3,550</td>
<td>-4%</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>Qualcomm (2)</td>
<td>U.S.</td>
<td>4,434</td>
<td>3,337</td>
<td>-25%</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>SK Hynix</td>
<td>South Korea</td>
<td>4,380</td>
<td>3,063</td>
<td>-30%</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>Micron</td>
<td>U.S.</td>
<td>4,061</td>
<td>2,930</td>
<td>-28%</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>TI</td>
<td>U.S.</td>
<td>2,940</td>
<td>2,804</td>
<td>-5%</td>
</tr>
<tr>
<td>9</td>
<td>10</td>
<td>Toshiba</td>
<td>Japan</td>
<td>2,619</td>
<td>2,446</td>
<td>-7%</td>
</tr>
<tr>
<td>10</td>
<td>9</td>
<td>NXP*</td>
<td>Europe</td>
<td>2,636</td>
<td>2,224</td>
<td>-16%</td>
</tr>
<tr>
<td>11</td>
<td>12</td>
<td>Infineon</td>
<td>Europe</td>
<td>1,666</td>
<td>1,776</td>
<td>7%</td>
</tr>
<tr>
<td>12</td>
<td>13</td>
<td>MediaTek (2)</td>
<td>Taiwan</td>
<td>1,506</td>
<td>1,691</td>
<td>12%</td>
</tr>
<tr>
<td>13</td>
<td>11</td>
<td>ST</td>
<td>Europe</td>
<td>1,700</td>
<td>1,601</td>
<td>-6%</td>
</tr>
<tr>
<td>14</td>
<td>14</td>
<td>Renesas</td>
<td>Japan</td>
<td>1,470</td>
<td>1,415</td>
<td>-4%</td>
</tr>
<tr>
<td>15</td>
<td>17</td>
<td>Apple (2)**</td>
<td>U.S.</td>
<td>1,260</td>
<td>1,390</td>
<td>10%</td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td>GlobalFoundries (1)*</td>
<td>U.S.</td>
<td>1,436</td>
<td>1,360</td>
<td>-5%</td>
</tr>
<tr>
<td>17</td>
<td>20</td>
<td>Nvidia (2)</td>
<td>U.S.</td>
<td>1,118</td>
<td>1,285</td>
<td>15%</td>
</tr>
<tr>
<td>18</td>
<td>16</td>
<td>Sony</td>
<td>Japan</td>
<td>1,272</td>
<td>1,125</td>
<td>-12%</td>
</tr>
<tr>
<td>19</td>
<td>18</td>
<td>UMC (1)</td>
<td>Taiwan</td>
<td>1,140</td>
<td>1,034</td>
<td>-9%</td>
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<tr>
<td>20</td>
<td>21</td>
<td>AMD (2)</td>
<td>U.S.</td>
<td>1,030</td>
<td>832</td>
<td>-19%</td>
</tr>
</tbody>
</table>

**Top 20 Total**

<table>
<thead>
<tr>
<th>Tot 20 Total</th>
<th>Tot 20 Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>66,745</td>
<td>62,440</td>
</tr>
</tbody>
</table>

### Notes:

- (1) Pure play foundry
- (2) Fabless supplier
- * Includes Intel/Altera, Avago/Broadcom, NXP/Freescale, and GlobalFoundries/IBM sales for 1Q15 and 1Q16.
- **Custom processors for internal use made by TSMC and Samsung foundry services.

Source: Companies, IC Insights' Strategic Reviews Database
### 2013/2014 Top 20 in TW

<table>
<thead>
<tr>
<th>Rank</th>
<th>Company</th>
<th>2014</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>聯發科</td>
<td>213,062,916</td>
<td>136,055,954</td>
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<tr>
<td>2</td>
<td>聯詠</td>
<td>54,066,983</td>
<td>41,449,655</td>
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<tr>
<td>3</td>
<td>群聯</td>
<td>33,074,698</td>
<td>32,174,331</td>
</tr>
<tr>
<td>4</td>
<td>瑞昱</td>
<td>31,263,298</td>
<td>28,180,009</td>
</tr>
<tr>
<td>5</td>
<td>奇景光電</td>
<td>25,391,000</td>
<td>22,867,800</td>
</tr>
<tr>
<td>6</td>
<td>擎亞</td>
<td>14,238,941</td>
<td>9,980,236</td>
</tr>
<tr>
<td>7</td>
<td>立鈞</td>
<td>11,930,118</td>
<td>10,728,649</td>
</tr>
<tr>
<td>8</td>
<td>弈力</td>
<td>10,049,614</td>
<td>9,628,257</td>
</tr>
<tr>
<td>9</td>
<td>旭曜</td>
<td>9,892,675</td>
<td>9,362,444</td>
</tr>
<tr>
<td>10</td>
<td>旭豪</td>
<td>9,794,664</td>
<td>6,190,638</td>
</tr>
<tr>
<td>11</td>
<td>凌陽</td>
<td>8,712,746</td>
<td>8,521,868</td>
</tr>
<tr>
<td>12</td>
<td>瑞鼎</td>
<td>8,093,151</td>
<td>10,211,043</td>
</tr>
<tr>
<td>13</td>
<td>義隆</td>
<td>7,686,322</td>
<td>7,794,533</td>
</tr>
<tr>
<td>14</td>
<td>鈊創</td>
<td>7,609,254</td>
<td>6,094,130</td>
</tr>
<tr>
<td>15</td>
<td>矢創</td>
<td>7,595,150</td>
<td>5,728,484</td>
</tr>
<tr>
<td>16</td>
<td>創意</td>
<td>6,952,281</td>
<td>6,176,741</td>
</tr>
<tr>
<td>17</td>
<td>威盛</td>
<td>6,494,965</td>
<td>6,095,973</td>
</tr>
<tr>
<td>18</td>
<td>智原</td>
<td>5,743,172</td>
<td>6,947,553</td>
</tr>
<tr>
<td>19</td>
<td>原相</td>
<td>4,749,080</td>
<td>4,628,579</td>
</tr>
<tr>
<td>20</td>
<td>揚智</td>
<td>4,647,395</td>
<td>4,155,584</td>
</tr>
<tr>
<td>21</td>
<td>致新</td>
<td>3,941,557</td>
<td>3,909,592</td>
</tr>
<tr>
<td>22</td>
<td>盛群</td>
<td>3,930,519</td>
<td>3,894,361</td>
</tr>
<tr>
<td>23</td>
<td>松翰</td>
<td>3,553,363</td>
<td>3,642,339</td>
</tr>
<tr>
<td>24</td>
<td>茂達</td>
<td>3,486,008</td>
<td>3,043,596</td>
</tr>
<tr>
<td>25</td>
<td>聯陽</td>
<td>3,440,965</td>
<td>3,561,112</td>
</tr>
</tbody>
</table>
## 2013~15 Top Packaging Houses

### Revenue of Global Top24 Packaging & Test Vendors, 2013-2015E

<table>
<thead>
<tr>
<th></th>
<th>2013</th>
<th>2014</th>
<th>2015E</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASE</td>
<td>4,740</td>
<td>5,288</td>
<td>6,082</td>
</tr>
<tr>
<td>AMKOR</td>
<td>2,956</td>
<td>3,129</td>
<td>3,380</td>
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<tr>
<td>SPIL</td>
<td>2,345</td>
<td>2,735</td>
<td>2,980</td>
</tr>
<tr>
<td>STATS ChipPAC (Acquired by JECT)</td>
<td>1,599</td>
<td>1,586</td>
<td>1,508</td>
</tr>
<tr>
<td>PTI</td>
<td>1,270</td>
<td>1,318</td>
<td>1,320</td>
</tr>
<tr>
<td>J-devices</td>
<td>908</td>
<td>920</td>
<td>930</td>
</tr>
<tr>
<td>UTAC</td>
<td>748</td>
<td>734</td>
<td>785</td>
</tr>
<tr>
<td>JECT</td>
<td>775</td>
<td>1,046</td>
<td>1,302</td>
</tr>
<tr>
<td>ChipMOS</td>
<td>649</td>
<td>696</td>
<td>670</td>
</tr>
<tr>
<td>Chipbond</td>
<td>534</td>
<td>537</td>
<td>540</td>
</tr>
<tr>
<td>KYEC</td>
<td>496</td>
<td>536</td>
<td>600</td>
</tr>
<tr>
<td>STS Semiconductor</td>
<td>499</td>
<td>530</td>
<td>590</td>
</tr>
<tr>
<td>Huatian Technology</td>
<td>395</td>
<td>538</td>
<td>610</td>
</tr>
<tr>
<td>MPI (Carsem)</td>
<td>389</td>
<td>400</td>
<td>376</td>
</tr>
<tr>
<td>Nepes</td>
<td>296</td>
<td>261</td>
<td>302</td>
</tr>
<tr>
<td>FATC</td>
<td>303</td>
<td>303</td>
<td>330</td>
</tr>
<tr>
<td>Walton</td>
<td>300</td>
<td>330</td>
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<tr>
<td>Unisem</td>
<td>315</td>
<td>317</td>
<td>352</td>
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<tr>
<td>Nantong Fujitsu Microelectronics</td>
<td>285</td>
<td>340</td>
<td>385</td>
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<tr>
<td>Hana Micron</td>
<td>253</td>
<td>279</td>
<td>310</td>
</tr>
<tr>
<td>Signetics</td>
<td>254</td>
<td>223</td>
<td>190</td>
</tr>
<tr>
<td>Lingsen</td>
<td>204</td>
<td>195</td>
<td>185</td>
</tr>
</tbody>
</table>
2016 WW 12” fab

1. Samsung 22%
2. Micron 14%
3. TSMC 13%
4. 海力士 13%
......
8. UMC 3%
9. 力晶 2%

Taiwan vs. China
國際半導體協會（SEMI）2016 Dec. 數據預估，2017 年到 2020 年未來四年將有 62 座新晶圓廠投產，其中將有四成晶圓廠共 26 座新晶圓廠座落中國，美國將有 10 座位居第二，台灣估計也會有 9 座。SEMI 估計，新晶圓廠中將有 32% 用於晶圓製造、21% 生產記憶體、11% 與 LED、MEMS、光學、邏輯與類比晶片等相關。
Taiwan

Source: Industry & Technology Intelligence Service, MOE, 2007/04
Taiwan